configurations, and timing mechanisms may be provided without departing from the teachings provided herein. In addition, one or more blocks of one flow diagram may be combined with one or more blocks of another diagram.

[0067] It is also imperative to note that all of the Specifications, protocols, and relationships outlined herein (e.g., specific commands, timing intervals, supporting ancillary components, etc.) have only been offered for purposes of example and teaching only. Each of these data may be varied considerably without departing from the spirit of the present disclosure, or the scope of the appended claims. The specifications apply to many varying and non-limiting examples and, accordingly, they should be construed as such. In the foregoing description, example embodiments have been described. Various modifications and changes may be made to such embodiments without departing from the scope of the appended claims. The description and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

[0068] Numerous other changes, substitutions, variations, alterations, and modifications may be ascertained to one skilled in the art and it is intended that the present disclosure encompass all such changes, substitutions, variations, alterations, and modifications as falling within the scope of the appended claims. In order to assist the United States Patent and Trademark Office (USPTO) and, additionally, any readers of any patent issued on this application in interpreting the claims appended hereto, Applicant wishes to note that the Applicant: (a) does not intend any of the appended claims to invoke paragraph six (6) of 35 U.S.C. section 112 as it exists on the date of the filing hereof unless the words "means for" or "step for" are specifically used in the particular claims; and (b) does not intend, by any statement in the Specification, to limit this disclosure in any way that is not otherwise reflected in the appended claims.

EXAMPLE EMBODIMENT IMPLEMENTATIONS

[0069] One particular example implementation may include an apparatus for managing power for at least one processor that includes means for evaluating (e.g., via a processor, software, circuitry, a hub, a controller, etc.) a plurality of ports associated with an electronic device; means for determining that a particular pin associated with at least one of the ports is not receiving a signal; means for disabling a squelch function associated with the electronic device; and means for gating power (e.g., over any suitable interface, link, bus, communication pathway, etc.) associated with a physical layer (PHY) of the electronic device.

[0070] Another particular example may include an apparatus for managing power for at least one processor that includes means for identifying (e.g., via a processor, software, circuitry, a hub, a controller, etc.) a power management event (PME) timeout; means for (e.g., via a processor, software, circuitry, a hub, a controller, etc.) directing a receiver in a physical layer (PHY) to turn off; means for transitioning from a powered-on link state to a recovery state; and means for resuming a detection state associated with a predetermined timeout associated with failing to receive a sequence from the electronic device.

[0071] Still another example embodiment may include an apparatus for managing power for at least one processor that includes means for providing a configuration bit of a root port; means for initiating (e.g., via a processor, software, circuitry, a hub, a controller, etc.) a power management event turn off/acknowledgment handshake signal for the root port for putting a corresponding link into layer 2/layer 3 (L2/L3) ready state; means for instructing (e.g., via a processor, software, circuitry, a hub, a controller, etc.) a power management controller (PMC) to assert a reset for the electronic device; and means for removing power such that the electronic device transitions to a cold state.

1.-9. (canceled)

10. A system, comprising:

a processor; and

a memory to store instructions that when executed by the processor performs operations, comprising:

identifying a power management event (PME) timeout;

directing a receiver in a physical layer (PHY) to turn off;

transitioning from a powered-on link state to a recovery state; and

resuming a detection state associated with a predetermined timeout associated with failing to receive a sequence from the electronic device.

11. The system of claim **10**, wherein incoming data is cut off from the electronic device in response to the PHY being turned off.

12. The system of claim **10**, wherein the detection state is resumed before indicating a layer 2/layer 3 (L2/L3) ready state for the electronic device.

13. The system of claim **10**, wherein the detection state is resumed before clearing a runtime-entry configuration bit for the electronic device.

14. The system of claim **10**, wherein a runtime element is used to enable the PHY to be power gated.

15. The system of claim **10**, wherein a receiver termination remains enabled and a transmitter common mode is turned off as the PHY is power gated.

16. The system of claim **10**, wherein power is to be removed from the electronic device such that the electronic device resides in a device power state and a root port remains in a system working state.

17.-30. (canceled)

* * * * *